What is claimed is:

1. A semiconductor package, comprising:

a semiconductor chip provided with a plurality of bond pads on its upper surface;

a chip paddle adjacent a bottom surface of said semiconductor chip;

a plurality of internal leads surrounding said chip paddle;

conductive wires for electrically connecting said bond pads of said semiconductor chip to said internal leads; and

a package body comprised of encapsulation material that encapsulates said semiconductor chip, said conductive wires, said chip paddle and said internal leads, wherein said chip paddle and said internal leads are externally exposed at a bottom surface of said chip paddle and said internal leads.

2. The semiconductor package as set forth in claim 1, wherein:

a lower side area of said chip paddle has an etched part wherein the etched part is about 10% to about 90 % of said lower side area of said chip paddle, and said etched part is located inside said package body.

3. The semiconductor package as set forth in claim 2, wherein:

said chip paddle and a lower surfaces of said internal leads are in a common plane, and wherein said chip paddle is thicker than said internal leads.

4. The semiconductor package as set forth in claim 1, wherein: said chip paddle and a lower surfaces of said internal leads are in a common plane, and wherein said chip paddle is thicker than said internal leads.

5. The semiconductor package as set forth in claim 1, wherein:

said chip paddle is bonded to a bottom surface of said semiconductor chip with an adhesive.

6. The semiconductor package as set forth in claim 1, wherein:

each of said internal leads have an etched part at an end facing said chip paddle.

7. The semiconductor package as set forth in claim 1, wherein:

said internal leads are externally exposed at their side surfaces and bottom surfaces.

8. A method of increasing a moisture path in a semiconductor package comprising the steps of:

providing a chip paddle;

providing a plurality of internal leads surrounding said chip paddle;

locating a semiconductor chip on said chip paddle;

electrically connecting said semiconductor chip to said internal leads with conductive wires;

encapsulating said semiconductor chip, said conductive wires, said chip paddle and said internal leads, with encapsulation material, wherein said chip paddle and said internal leads are externally exposed at a bottom surface of said chip paddle and said internal leads; and

etching a lower side area of said chip paddle wherein the etched part is about 10% to about 90 % of a lower side area of said chip paddle and wherein said etched part is located inside said encapsulation material.

9. The method according to claim 8, further comprising the step of:

placinga lower surface of said chip paddle and a lower surface of said internal leads in a common plane.

10. The method according to claim 8, further comprising the step of:

bonding said chip paddle to a bottom surface of said semiconductor chip with an adhesive.

11. The method according to claim 8, wherein:

said step of encapsulating said chip paddle and said internal leads includes externally exposing said internal leads at a side surface and a bottom surface of said leads.

12. The method according to claim 8, wherein:

said steps are sequential.

13. A packaged semiconductor, comprising:

a chip paddle adapted to receive a semiconductor chip;

a plurality of internal leads surrounding said chip paddle wherein said chip paddle and said leads comprise a leadframe; and

said leadframe adapted to receive a package body comprised of encapsulation material for encapsulating said chip paddle and said internal leads, wherein said chip paddle and said internal leads are externally exposed at a bottom surface of said chip paddle and said internal leads.

14. The packaged semiconductor as set forth in claim 13, wherein

a lower side area of said chip paddle has an etched part wherein the etched part is about 10% to about 90 % of said lower side area of said chip paddle, and said etched part is located inside said package body.

15. The packaged semiconductor as set forth in claim 14, wherein

said chip paddle and a lower surfaces of said internal leads are in a common plane, and wherein said chip paddle is thicker than said internal leads.

16. The packaged semiconductor as set forth in claim 13, wherein said chip paddle and a lower surfaces of said internal leads are in a common plane, and wherein said chip paddle is thicker than said internal leads.

17. The packaged semiconductor as set forth in claim 13, wherein:

each of said internal leads have an etched part at an end facing said chip paddle.

18. The packaged semiconductor as set forth in claim 13, wherein:

said internal leads are externally exposed at their side surfaces and bottom surfaces.